Q.P. Code:16EC5704 **R16**

Reg. No. | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
M.Tech I Year I Semester Regular & Supplementary Examinations February 2018
VERILOG HDL
(VLSI)

Time: **3** hours Max. Marks:**60**

(Answer all Five Units **5 X 12 =60** Marks)

UNIT-I

1	a.	Explain structure design methodology with the verilog HDL.	7M
	b.	Write verilog HDC structural model for a full sub tractor using NAND gates.	5M

OR

2	a.	Explain about Arrays of Instances in verilog with an example.	7M
	b.	Write a brief notes on number representation in verilog.	5M

UNIT-II

3	a.	What is user defined primitives? Explain combinational behavior of user defined primitives	7M
	b.	Explain conditional operator, operator precedence in VERILOG.	5M

OR

4	a.	Compare the combinational behavior and sequential behavior of user defined primitives.	7M
	b.	Explain the following i) Inertial Delay Effects ii) Pulse Rejection	5M

UNIT-III

5	a.	Write a short note on intra assignment delay.	5M
	b.	Explain behavioral models of finite state machines.	7M

OR

6	a.	Draw the ASM chart for the dice game and write a program in behavioral models verilog HDL	7M
	b.	Explain the Procedural assignment statement.	5M

UNIT-IV

7	a.	Draw the block diagram for test bench for post synthesis design verifications.	7M
	b.	Discuss about behavioral synthesis.	5M

OR

8	a.	Draw the flow chart for synthesis of loops explain each block?	7M
	b.	Write program for synthesis of multi cycle operations	5M

UNIT-V

9	a.	Write and verify the switch level al JK flip flop having preset and clear input?	7M
	b.	Explain the following. a) Strength reduction by primitives. b) Transistor switch & bi-directional switch	5M

OR

10	a.	Write and verify a switch level al a three input static CMOS NOR gate?	7M
	b.	Explain the true table for switch level MOSFET transistor module?	5M

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